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### **Optimization of Pattern Matching Algorithm for Memory**

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### **Algorithm-Architecture Matching for Signal and Image**

put to this parallel data-path architecture is a complex problem. This thesis presents a memory architecture template that can be parameterized for a given FBM algorithm, number of parallel processing elements, and block size. The template can be parameterized with well known exploration techniques to design efficient on-chip memory subsystems.

### **MEMORY ARCHITECTURE TEMPLATE FOR FAST BLOCK MATCHING**

system must have a memory-efficient pattern-matching algorithm and hardware design. In this paper, we propose a memory-efficient pattern-matching algorithm which can significantly reduce the memory requirement. For total Snort string patterns, the new algorithm achieves 29% of memory reduction compared with the traditional Aho-Corasick ...

### **Optimization of Pattern Matching Algorithm for Memory**

string matching accelerator based on a memory implementation of the AC FSM. Tan et al. [27] proposed the

bit-split algorithm partitioning a large AC state machine into small state machines to significantly reduce the memory requirements. Jung et al. [14] presented an FPGA implementation of the bit-split string matching architecture.

### **Novel Pattern Matching using FSM Algorithm for Memory**

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